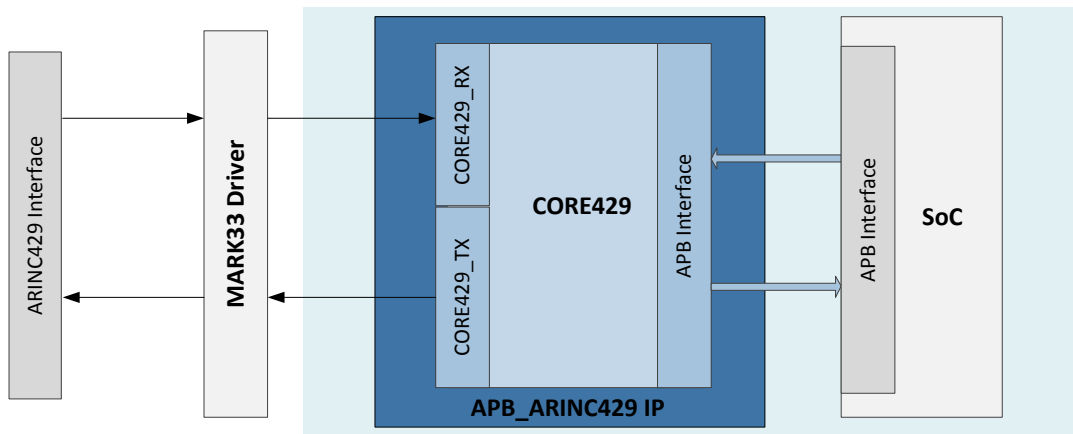




DO254-IP: APB/ARINC429

KEY FEATURES

- Developed according to DO-254/ED-80 guidance. Compliant DAL A.
- Compliant with ARINC 429 Protocol published on September 27, 2001.
- Compliant with AMBA 3 APB Protocol v1.0.
- Compliant with Mark 33 Digital Information Transfer System.
- Actel® Corporation property.



TECHNICAL FEATURES

- Clock frequency configurable in 1 MHz, 10 MHz, 16 MHz or 20 MHz
- 512 bytes of APB address space
- Rx and Tx ARINC429 Channels number independently configurable from 1 to 16
- ARINC429 input and output configurable in Low (12.5 kHz or 50 kHz) or High (100 kHz) speed mode
- One FIFO for each ARINC429 channel
- ARINC429 channel FIFO depth configurable in 32, 64, 128, 256 or 512 bits
- APB_ARINC429 IP supports up to 256 unique labels per Receive channel
- AMBA APB Read data bus width and Write data bus width configurable in 8, 16 or 32 bits
- A support Source/Direction Identifiers mechanism per Receive channel
- A loopback mode for safety and testing purpose
- Supporting the main Actel® device families (proASIC+, etc...)



OVERVIEW

The APB_ARINC429 module is an ARINC429 to APB Bridge. It allows a system with an embedded APB bus to be connected to an external ARINC429 interface. The hardware item only covers digital layers of the ARINC 429 Protocol bus architecture. With its unique internal architecture the digital core is optimized for low gate count and low latency applications. The APB_ARINC429 matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the DO-254/ED-80 guidelines.

This component has been developed, verified and licensed by DMAP.

DELIVERABLES

- Verilog RTL sources code compliant with DMAP's design standard.
- Verilog verification test-benches using a BFM, a data and configuration generator, a CPU and a score board to compare final result.
- Reference Design as integration example (Dry Run) on Actel® device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process:** Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards:** Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process:** Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
- **Hardware Verification and Validation Process:** Hardware Verification Cases Procedures (HVCP) and Hardware Verification Results (HVR) and validation activities reports.
- **Design Assurance Records:**
 - **Peer Reviews.**
 - **Design Reviews:** Initial Design Review (IDR), Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Design Review (FDR).
 - **Hardware Reviews:** Stage of Involvement (SOI) #1, #2, #3 and #4.
 - **Audits.**
- **Hardware Configuration Management Process:** Hardware Configuration Index (HCI), Hardware Environment Configuration Index (HECI).

CONTACT

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