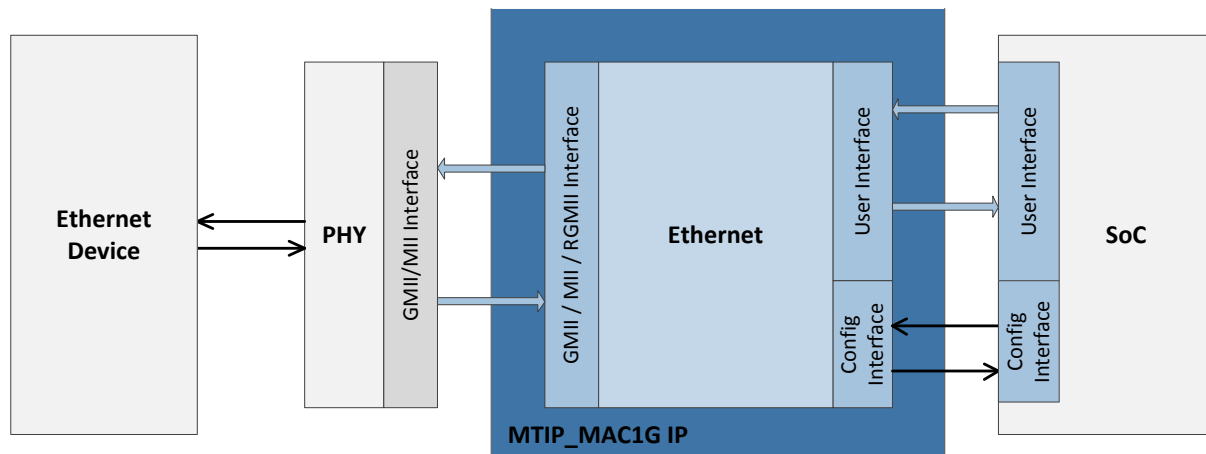




## DO254-IP: ETHERNET®

### KEY FEATURES

- Developed according to RTCA/DO-254 ED-80 guidance. Compliant DAL A
- Compliant with IEEE Std 802.3-2002 Ethernet Edition, IEEE 802.1Q-1998 Edition, UNH Certified.
- Simple FIFO User Interface.
- Compliant with GMII / MII IEEE Std 802.3, RFC2665 and RFC2863 ([www.ietf.org](http://www.ietf.org))
- MoreThanIP intellectual property ([www.morethanip.com](http://www.morethanip.com))



### TECHNICAL FEATURES

- Tri-Mode 10/100/1000 Fully integrated Ethernet MAC in Full-duplex.
- Supports Preamble, SFD and frame padding generation, CRC on both Rx and Tx path.
- Support for VLAN tagged frames according to IEEE 802.1Q and 9kB jumbo frame.
- Configurable to support 10Mbps, 100Mbps or 1Gbps operation.
- 32 bits simple FIFO interface to user application compatible with simple FIFO interface.
- User interface for Configuration Registers and status information (VLAN tag, frame type and errors).
- GMII (125MHz) or MII (25MHz) interface to Ethernet PHY device.
- Full report done to remote peer and to SoC. (Parity on data buffers, FSM monitoring).
- CRC-32 with optional forwarding of the FCS field.
- Autonomous and dynamically configurable XON/XOFF Pause Frame (802.3 Annex 31A) support.
- Optimized for low gate count (20k-40k gates) and low core latency. Technology independent (Altera/Xilinx/Actel/ASIC).
- Configurable buffer size from 64B to 16kB depending on performance requirement.
- Optional support of AMD Magic Packet detection for node remote power management.
- Support multiple MAC address filtering and multicast address filtering on Rx path with hash table.

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Design Methods & Assurance Process

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## OVERVIEW

The MTIP\_MAC1G module provides, with a single IP Core, a solution for Ethernet applications operating at 10/100 or 1Gbit. It allows a SoC to be connected to an external Ethernet Network. The hardware item only covers digital layers of the IEEE 802.3 MAC bus architecture. It supports transparent (for switching application) and full Ethernet frame handling for connected device. With its unique internal architecture the digital core is optimized for low gate count and low latency applications. For efficient power management, the core can implement the Magic Packets detection. The MTIP\_MAC1G is able to recover from SEU and to report any detected errors with the help of its embedded reliability features. Detected errors are then reported to external system and to internal sub-system. The MTIP\_MAC1G matches major needs of any critical application and mainly those which require a DO-254 DAL-A compliance in the aerospace area.

The development has been done according to the RTCA/DO-254 ED-80 guidelines.

This component has been developed, verified and licensed by DMAP.

## DELIVERABLES

- Verilog RTL sources code compliant with DMAP's design standard.
- SystemVerilog Functional verification test-benches using best-in class BFM from Mentor Graphics with full code and functional coverage.
- Reference Design as integration example (Dry Run) on Altera device.
- DMAP's support includes technical integration, DO-254 integration and certification phases.
- IP Datasheet and Customer Requirement Specification (CRS) document.

It includes all required data for RTCA/DO-254/ED-80 certification, including configuration management records, change management records and assurance process records:

- **Hardware Planning Process:** Hardware Development Plan (HDP), Hardware Validation and Verification Plan (HVVP), Hardware Configuration Management Plan (HCMP), Hardware Process Assurance Plan (HPAP) and Plan for Hardware Aspects of Certification (PHAC).
- **Standards:** Hardware Requirement Standard (HRS), Hardware Design Standard (HDS).
- **Hardware Development Process:** Hardware Requirement Document (HRD), Hardware Conceptual Document (HCD), Hardware Detailed Document (HDD), Hardware Traceability Matrixes (HTM), Hardware Accomplishment Summary (HAS) and Hardware Software Interface Document (HSID).
- **Hardware Verification and Validation Process:** Hardware Verification Cases Procedures (HVCP) and Hardware Verification Results (HVR) and validation activities reports.
- **Design Assurance Records:**
  - **Peer Reviews, Project Reviews:** Initial Design Review (IDR), Preliminary Design Review (PDR), Critical Design Review (CDR) and Final Design Review (FDR).
  - **Audits, Hardware Reviews:** Stage of Involvement (SOI) #1, #2, # 3 and #4.
- **Hardware Configuration Management Process:** Hardware Configuration Index (HCI), Hardware Environment Configuration Index (HECI).

## CONTACT

**Product Reference:** MTIP\_MAC1G.

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